CIO-DAC16
and
CIO-DAC08

User's Manual

Revision 4
October, 2000

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1 INTRODUCTION

The CIO-DAC16 is a 16 channel analog output board. The CIO-DAC08 is an eight channel analog output board. The analog outputs are dual-DAC AD7273s with each output buffered by an OP07. The CIO-DAC family is compatible with MetraByte's DDA-06 but lacks digital outputs. Software designed for the DDA-06 will operate the analog outputs.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. The control register is double buffered so the DAC's output is not updated until the second byte (the high byte) has been written.

The analog outputs can also be set for simultaneous update in groups of two, four, six, etc. or all sixteen. When a DAC pair is set for simultaneous update, writing new digital values to the DAC's control register does not cause an update of the DAC's voltage output. Update of the output occurs only after a READ from the board's addresses.

2 SOFTWARE INSTALLATION

An installation program labeled InstaCal™ is on the disk shipped with the board. This program will guide you through board configuration and switch settings. Refer to the *Extended Software Installation Manual* for complete instructions regarding installing and using *Insta*Cal. If you decide not to use *Insta*Cal as a guide, the information required for configuring the board is provided in the following section.

3 HARDWARE INSTALLATION

3.1 Initial Board Setup

The CIO-DAC## has one bank of gain switches for each analog output channel, one base address switch, a simultaneous update jumper for each DAC pair, a “power-up state” selection jumper and one wait state jumper block which must be set before installing the board in your computer. The *Insta*Cal calibration and test program included with the CIO-DAC## will show how these switches are to be set. Run the program before you open your computer.

The CIO-DAC## is setup at the factory as follows:

BASE ADDRESS	300h (768 decimal)
WAIT STATE	Off Position, Right
SIMULTANEOUS UPDATE	Single Channel Update
ANALOG OUTPUT	$\pm$5V
POWER UP STATE	Standard (undefined output values at power up)

3.2 Selecting the Base Address

Unless there is already a board in your system that uses address 300h (768 decimal), leave the switches as they are set at the factory.

In the example shown here, the CIO-DAC## is set for base address 300h (768 decimal).

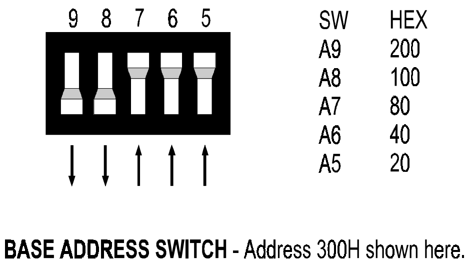


Figure 3-1. Base Address Switches

Certain address are used by the PC, others are free and can be used by the CIO-DAC## and other expansion boards. We recommend you try the factory default BASE = 300h (768 decimal) first.

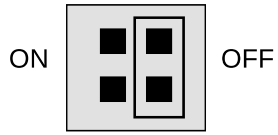
Table 3-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC#1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BB	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-DAC## BASE switch can be set for address in the range of 000-3E0 so it should not be hard to find a free address area for you CIO-DAC##. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use. Address not specifically listed, such as 390-39F, are free.

3.3 Wait State Jumper

The CIO-DAC## boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DAC## board so that signals from slow devices (chips) will be valid.



WAIT STATE JUMPER BLOCK - This block has no wait state selected. For a wait state, place the jumper on the two leftmost pins.

Figure 3.2. Wait State Jumper

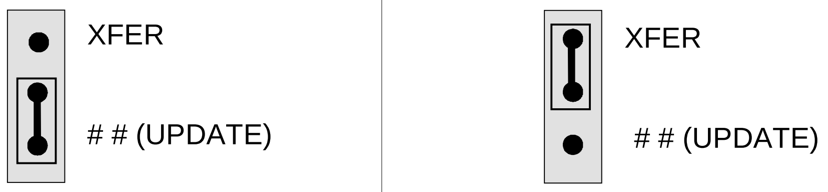
The wait state generator on the CIO-DAC## is only active when the CIO-DAC## is being accessed. Your PC will not be slowed down in general by using the wait state.

3.4 Individual / Simultaneous Update Jumpers

Analog outputs can be jumpered so that new output data is held until one or more DACs have been loaded with new digital data. Then, as a group, the new data transfers to the voltage outputs. The simultaneous transfers occurs when any of the CIO-DAC## addresses are read (and the jumpers are in the “XFER” position).

The analog output chips on the CIO-DAC## are dual DACs (two analog outputs per chip). A single jumper sets both DACs on a single chip to be either simultaneously transferred on a read (XFER) or the ouputs are individually updated when the MSB register is written.

The diagram below shows the jumper block in each mode. If you look on the CIO-DAC## board, you will see numbers such as 12, 34, 56... (reading right to left) below each jumper. The numbers indicate the pair of channels that the jumper selects.



Individual updates per DAC
(Two Channels)

Simultaneous updates from all DACs
Jumpered to XFER

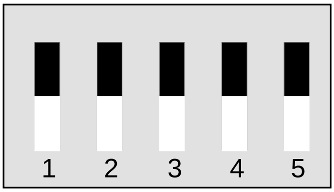
INDIVIDUAL UPDATE / SIMULTANEOUS TRANSFER JUMPER
J1 to J8 - One per pair of channels.

Figure 3-3. Simultaneous Update Jumper

3.5 Analog Output Range Switches

The analog output voltage range of each channel can be set with a set of five ganged DIP switches. The switch blocks are located on the board below the calibration potentiometers. The switch blocks are labeled 0 to 15 (0 to 7 on the CIO-DAC08) and individual switches are labeled 1 through 5.

Set the switches for each individual channel as shown in Figure 3-4..



RANGE					
+/-10V	UP	DN	UP	DN	DN
+/-5V	UP	DN	DN	UP	DN
+/-2.5V	UP	DN	DN	DN	UP
0 to 10V	DN	UP	UP	DN	DN
0 to 5V	DN	UP	DN	UP	DN
0 to 2.5V	DN	UP	DN	DN	UP

Figure 3-4. Output Range Switch

To set a channel to a particular range, read the switch positions as UP or DN (down) from left to right in the row beside the range you desire.

For example, the ±5V range is: UP>DN>DN>UP>DN.

3.6 Installing the CIO-DAC## in the Computer

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it can fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAC##.

3.7 Cabling to the CIO-DAC##

The CIO-DAC## connector is accessible through the PC/AT expansion bracket. The connector is a standard 37-pin male connector. A mating female connector, such as the C37FF-2, is available from OMEGA.

Several cabling and screw termination options are available from OMEGA.

DFCON-37	D connector, D shell and termination pins to construct your own cable
C37FF-2	2-foot (and longer) ribbon cable with 37 pin D connectors
C37FFS-5	5-foot shielded round cable with molded ends housing 37-pin connectors. Also available in 10-ft. length.
CIO-MINI37	Simple, 40-position 4”X4” screw terminal board
CIO-TERMINAL	Full featured 4 x 16 in. screw terminal board with prototyping and interface circuitry

3.8 Testing the Installation

You can test the installation of the CIO-DAC## using InstaCal. Select the Test option to vary the output voltages and monitor them with a Volt Meter.

3.9 Signal Connection

The analog outputs of the CIO-DAC## are two-wire hookups. A signal, labeled D/A # OUT on the connector diagram below, and a Low Level Ground (LLGND). The low level ground is an analog ground and is the ground reference which should be used for all analog hookups.

Possible analog output ranges are:

Bipolar Ranges	±10V	±5V	±2.5V
	and		
Unipolar Ranges	0 to 10V	0 to 5V	0 to 2.5V

See the range select switch in section 3.5.

Each of the DAC## outputs are individually buffered through an OP07 operational amplifier (OP-AMP). The OP07s are socketted so that if one fails it can be replaced in the field. The OP07 for each channel is located just below the calibration potentiometers for that channel.

At the full rated output swing of ±10V, each channel is capable of sinking or sourcing ±5 mA. That means a load of 2K Ohms can be connected to each channel.

As the load resistance is raised from 2K up to 10 Megaohms or more, the output load on the DAC decreases. Any load resistance greater than 2K is fine.

As the load resistance decreases, the output load increases. The OP07 responds by producing a lower output voltage. If your CIO-DAC## will not produce the output voltage specified by the code & range combination, it is a good idea to check the load with an ohm meter.

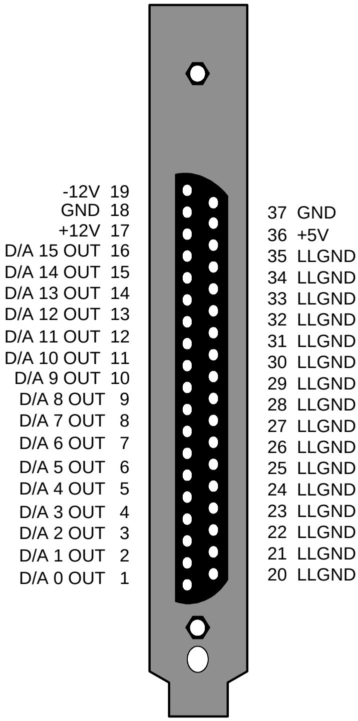
Under normal circumstances you will not damage the OP07 by connecting the output to ground. If your connection results in a failure of the OP07, chances are good that there was some potential at the connecting point in addition to a load at ground or between 0 and 2K ohms. Explore the point with a DVM before reconnecting the CIO-DAC## (and after replacing the OP07 of course). Connect the negative lead of the DVM to any LLGND pin of the CIO-DAC##.

3.10 Connector Diagram

The CIO-DAC## connector is a 37-pin D-type connector accessible from the rear of the PC through the expansion backplate.

The connector accepts female 37-pin D type connectors, such as those on the C37FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, refer to the information on the CIO-TERMINAL, CIO-SPADE50 and CIO-MINI37 screw terminal boards.



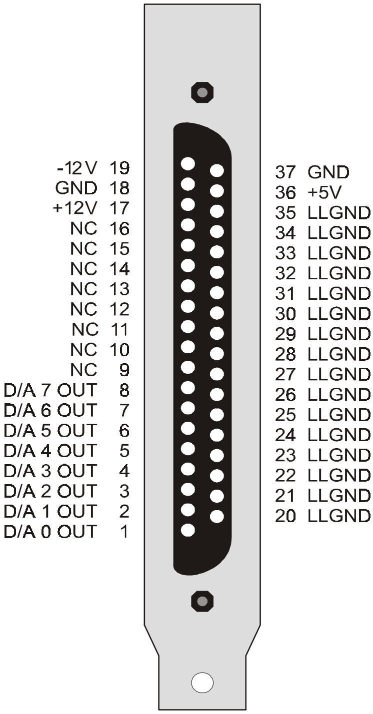


Figure 3-5.. Connector CIO-DAC16 Figure 3-6. Connector CIO-DAC08

4 REGISTER ARCHITECTURE

The CIO-DAC## is a simple board to understand. All control and data is read/written with simple I/O read and write commands. No interrupt or DMA control software is required. Thus, the board's functions are easy to control directly from BASIC, C or PASCAL.

4.1 Control & Data Registers

The CIO-DAC16 has 32 analog output registers, the CIO-DAC08 has 16. There are two registers for each channel; one for the lower 8 bits and one for the upper 4 bits.

The first address, or BASE ADDRESS, is determined by the setting of a bank of switches on the board.

The register descriptions all follow the format:

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

Table 4-1. Register Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming to set or read bits from bytes is beyond the scope of this manual. It is covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed in the following table. Each register has eight bits which can constitute a byte of data or eight individual read/write functions. The CIO-DAC08 has 8 pairs of register (Base + 0 through Base + 15) and the CIO-DAC16 has 16 pairs of register (Base + 0 through Base + 31).

Table 4-2. Register Map

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Intiate simultaneous update
BASE + 1	D/A 0 Most Significant Nibble	Intiate simultaneous update
BASE + 2	D/A 1 Least Significant Byte	Intiate simultaneous update
BASE + 3	D/A 1 Most Significant Nibble	Intiate simultaneous update
BASE + 4	D/A 2 Least Significant Byte	Intiate simultaneous update
BASE + 5	D/A 2 Most Significant Nibble	Intiate simultaneous update
BASE + 6	D/A 3 Least Significant Byte	Intiate simultaneous update
BASE + 7	D/A 3 Most Significant Nibble	Intiate simultaneous update
BASE + 8	D/A 4 Least Significant Byte	Intiate simultaneous update
...		
BASE + ##	And so on for each DAC	Same

The DAC16 contains 32 registers (16 register pairs). The DAC08 contains 16 registers. Each register-pair controls one D/A output.

Each DAC has two 8-bit registers which are used to control it. The first register contains the least significant eight bits of D/A code and should be written *first*.

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12 (LSB)

The second register contains the most significant four bits of D/A code and should be written to *second*. A write to this register updates the output of the D/A with all 12 bits of the D/A code contained in the two registers. If the XFER jumper is set for the DAC, no update will occur until a read of any one of the DAC registers is executed. Upon a read, all DACs set for simultaneous update (XFER jumper set) will update together.

7	6	5	4	3	2	1	0
X	X	X	X	D1 (MSB)	D2	D3	D4

4.2 Output Transfer Functions

To program a DAC, you must select the output you desire in volts, then apply a transfer function to that value. The transfer function for code = output is:

The UNIPOLAR transfer function of the DAC is:

FSV / 4096 * CODE = OutV or CODE = OutV / FSV * 4096

For Example:
If the range is 0 to 5V, and you desire a 2V output CODE = 2/5 * 4096
CODE = 1638

The BIPOLAR transfer function for the DAC is:

FSV/4096 * CODE - 0.5 * FSV or CODE = (OutV + 0.5 * FSV) / FSV * 4096

For example:
If the range is set to ±10 and you desire a −7V output
CODE = (−7V + 0.5 * 20) / 20 * 4096
CODE = 614

5 SPECIFICATIONS

POWER CONSUMPTION

CIO-DAC16	
+5V supply	435 mA typical, 525 mA max
+12V supply	140 mA typical, 180 mA max
−12V supply	80 mA typical, 105 mA max
CIO-DAC08	
+5V supply	435 mA typical, 525 mA max
+12V supply	75 mA typical, 98 mA max
−12V supply	52 mA typical, 68 mA max

ANALOG OUTPUT

D/A type	AD7237
Resolution	12 bits
Number of channels	
CIO-DAC16	16 Voltage Outputs
CIO-DAC08	8 Voltage Outputs
Output Ranges	±10V, ±5V, ±2.5V, 0 to 10V, 0 to 5V, 0 to 2.5V. Each channel independently switch-selectable.
D/A pacing	Software paced
Data transfer	Software
Offset error	Adjustable to zero
Gain error	Adjustable to zero
Differential non-linearity	±½ LSB max
Integral non-linearity	±½ LSB max
Monotonicity	12 bits
Gain drift (DAC)	±30 ppm/°C max
Offset drift (DAC)	±3 ppm/°C max
Throughput	System-dependent
Slew Rate	0.3 V/µs Typical
Settling time (20V step to .01%)	70 µs
Current Drive	±5 mA min
Output short-circuit duration	Indefinite
Output coupling	DC
Output resistance (OP-07)	0.1 ohm max
Miscellaneous	Double-buffered output latches

Update DACs individually or simultaneously (jumper-selectable by pairs)
DAC output state on power up and reset undefined

ENVIRONMENTAL

Operating temperature range	0 to 70°C
Storage temperature range	–40 to 100°C
Humidity	0 to 90% non-condensing

For your notes.

EC Declaration of Conformity

Part Number	Description
CIO-DAC16	16 Channel analog output board
CIO-DAC08	8 Channel analog output board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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